Research Statement

My current research focus includes computer architecture, high performance computing (HPC), embedded systems, HPC in healthcare technology, and performance and power evaluation. I have been conducting innovative research to develop power-aware HPC systems since I was a PhD student at Florida Atlantic University (FAU). As a principle investigator (PI) at Wichita State University (WSU), I have received eight research grants from external agencies including National Science Foundation (NSF), NVIDIA Corporation, and NetApp, Inc. I also have received two research grants from the WSU internal sources. I have published more than 14 refereed journal articles, two book chapters, more than 54 peer-reviewed conference papers, and more than ten technical articles out of my research work. I have been serving the research communities as a panel reviewer, panel presenter, invited speaker, journal reviewer, technical/international program committee member, and numerous volunteer activities inside/outside my university.

In my Computer Architecture and Parallel Programming Laboratory (CAPPLab) at WSU, recently I have been involved with two important research projects: (i) Discovering HPC-based digital mammography techniques for early detection and analysis of breast cancer (funded by the Flossie E. West Memorial Foundation) and (ii) designing a communication-aware multicore/ many-core systems with wireless routers to achieve energy-efficient scalable performance (partially funded by NVIDIA). In these projects, our primary contributions include (i) converting mammogram images into equivalent digital values and (ii) developing/applying novel data and task regrouping based multithreaded parallel algorithms to solve various big data problems. After successful completion of these projects, there will be new time- and cost-effective solutions for early detection and fast analysis of breast cancer. Research outcomes of this project can be applied to prevent and control other types of cancer such as lung cancer and skin cancer.

I was first involved with academic research activities during my undergraduate study at Bangladesh University of Engineering and Technology (BUET), an ABET accredited institution. I developed a computer simulation platform using FORTRAN language to facilitate *"Computer Aided Design of Batwing Antenna Arrays by Standing Wave Modeling of Current Distribution"*. This work was published at BUET as a Technical Report and it was accepted in partial fulfillment of the requirements for the BS degree in Electrical Engineering. I was so inspired by my undergraduate research work that I decided to go with Thesis option for my MS degree in Computer Engineering at Florida Atlantic University (FAU).

My MS Thesis *evaluates memory latency of cluster-based cache-coherent multiprocessor systems with different interconnection topologies*. We focus on a cluster-based architecture which is a variation of Stanford DASH architecture. In this architecture, snoopy protocol is used inside each cluster (as the number of processors per cluster is small). Clusters are connected using directory-based scheme through an interconnection network to make the system scalable. Trace-driven simulation has been developed using three different network topologies (ring, mesh, and hypercube). The overall memory latency has been evaluated by running a representative set of SPLASH-2 applications. Simulation results show that the cluster-based multiprocessor system with hypercube topology outperforms those with mesh and ring topologies. This work is published in the Journal of Computers & Electrical Engineering.

My PhD dissertation *"Cache Optimization for Real- Time Embedded Systems"* demonstrates several effective solutions to select the right cache parameters to improve performance, decrease total power consumption, and significantly enhance execution time predictability. Our proposed Miss Table based cache locking scheme with victim cache is proven to be very effective for both single-core and multicore high performance computer architectures running real-time applications. In this research work, we show that even though fundamentally memory is slower than the processing core and power-hungry cache introduces additional unpredictability, various techniques including cache locking and cache optimization can be implemented to improve the performance and make the system more predictable and power-efficient.

During my graduate studies, I worked on two Motorola-FAU Research Grants – Executable process Flow and One Pass to Production under the supervision of my PhD advisor. We developed simulation platform to evaluate embedded architectures for Motorola iDEN Group. We presented our work at Motorola and various conferences. Our work was appreciated by Motorola and was published in various journals (including MTAP and MICPRO) and conference proceedings (sponsored by IEEE and SCS). I presented part of my research work in the 2005 FAU Graduate Research Competition and stood first (in oral presentation).

At WSU, currently I have been serving as the PI of NetApp NSF Connector project (2015-2016). My responsibilities in this NetApp project include developing a Network File Server (NFS) Connector for Apache Spark systems and integrating project findings into educational materials. Previously, I served as the PI of Kansas NSF EPSCoR First Award (2013-2014). My responsibilities included inventing novel task/data regrouping-based parallel solutions for multicore systems. The CUDA C/C++ parallel programming solutions developed in this project are being used by Dr. Ramazan Asmatulu (WSU Department of Mechanical Engineering) and Mr. Mizan Rahman (CEO of M2SYS Technology). Other grants where I served as the PI include WSU URCA (2014-2015) and Wiktronics Embedded Systems Project (2014). I received the NVIDIA GPU Research Center at WSU award (2015) and NVIDIA CUDA Teaching Center at WSU award (2012). Through various grants, I have supported more than 25 graduate and undergraduate students. I have supervised three PhD, 14 MS Thesis, six MS Project, and eight undergraduate research students.

The continuous chase for high performance computing systems, capable of communicating, sensing, controlling, and monitoring, has made the contemporary computing systems exceedingly complex (with heterogeneous, parallel, concurrent, and distributed subsystems). The complexity comes from both hardware and software, making it difficult, but not impossible, to further improving the performance to power ratio. Due to its tremendous potential, multicore architecture is being deployed in all sorts of modern computing devices. Similarly, more applications are being developed using multithreading techniques. We are developing a model with a communication-aware cache-mediator suitable for multithreaded applications to investigate energy-efficient scalable performance of multicore/many-core systems.

In conclusion, I am eager to join as a tenured, associate professor at *Wichita State University*, where I can work hard with research projects, write proposals to bring grant money, and make significant contributions with researching, publishing, and supervising students. From 5 years from now, I picture myself as a distinguished research professor at *Wichita State University*.